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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,165	11/04/2003	Pierre Morin	02GR109854488	5541

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,165	MORIN ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/15/2006 has been entered. An action on the RCE follows.

2. The amendment filed on 12/23/2005 has been entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

4. Claims 12,14-16, 20, 22-24 and 32, 34-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Saitoh, Pub. No. US2003/0040158.

Regarding claim 12, Saitoh teaches (fig. 5) a semiconductor device comprising: a semiconductor substrate (1); at least one first MOS transistor (NMOS) and at least one second MOS transistor (PMOS) in the semiconductor substrate (1); a dielectric layer (19) on the at least one first MOS transistor (NMOS) and on the at least one second MOS transistor (PMOS); and a first etch stop layer (14) covering the at least

one first MOS transistor (NMOS) and having a first residual stress level (inherent property of the material 14); and a second etch stop layer (16) covering the at least one first MOS (NMOS) transistor and the at least one second MOS transistor (PMOS) and having a second residual stress level different than the first residual stress level (layer 14 has a tensile stress and layer 16 has a compressive stress and hence layers 14 and 16 have different residual stress levels, refer to paragraph 0088 and 0089).

Regarding claim 14, Saitoh teaches the entire claimed structure of claim 12 above including the dielectric layer (19) includes contact openings therethrough for providing electrical connection to the at least one first MOS transistor and to the at least one second MOS transistor (refer to paragraph [0106]).

Regarding claim 15, Saitoh teaches the entire claimed structure of claim 12 above including the at least one first MOS transistor comprises NMOS transistor and the at least one second MOS transistor comprises PMOS transistor (fig. 4), and wherein the first and second etch-stop layers have opposite residual stress levels (refer to paragraph [0088] and [0089]).

Regarding claim 16, Saitoh teaches the entire claimed structure of claim 12 above including the first etch stop layer (14) has a positive residual stress (tensile stress) level above the NMOS transistor, and the second etch stop layer has a negative residual stress (compressive stress) level above the PMOS transistor (refer to paragraph [0088] and [0089]).

Regarding claim 20, Saitoh teaches (fig. 5) a semiconductor device comprising: a semiconductor substrate (1); at least one first NMOS transistor (NMOS) and at least

one second PMOS transistor (PMOS) in the semiconductor substrate (1); a dielectric layer (19) on the at least one first MOS transistor (NMOS) and on the at least one second MOS transistor (PMOS); a first etch stop layer (14) covering the at least one first NMOS transistor (NMOS) and having a first residual stress level (inherent property of the material); and a second etch stop layer (16) covering the at least one first NMOS (NMOS) transistor and the at least one second PMOS transistor (PMOS) and having a second residual stress level different than the first residual stress level (layer 14 has a tensile stress and layer 16 has a compressive stress and hence layers 14 and 16 have different residual stress levels, refer to paragraph 0088 and 0089).

Regarding claim 22, Saitoh teaches (fig. 1) the entire claimed structure of claim 12 above including the dielectric layer (19) includes contact openings therethrough for providing electrical connection to the at least one first NMOS transistor and to the at least one second PMOS transistor (refer to paragraph [0106]).

Regarding claim 23, Saitoh teaches the entire claimed structure of claim 12 above including wherein the first and second etch-stop layers have opposite residual stress levels (refer to paragraph [0088] and [0089]).

Regarding claim 24, Saitoh teaches the entire claimed structure of claim 20 above including the first etch stop layer has a positive residual stress (tensile stress) level above the at least one NMOS transistor, and the second etch stop layer has a negative residual stress (compressive stress) level above the at least one PMOS transistor (refer to paragraph [0088] and [0089]).

Regarding claim 32, Saitoh teaches (fig. 5, and paragraph [0113]-[0120]) a method for fabricating a semiconductor device comprising: forming at least one first MOS (NMOS) transistor and at least one second MOS (PMOS) transistor in a semiconductor substrate (1); forming a dielectric layer (19) on the at least one first MOS (NMOS) transistor and on the at least one second MOS (PMOS) transistor; and forming a first etch-stop layer (14) covering the at least one first MOS (NMOS) transistor and having a first residual stress level (inherent property of the material); and forming a second etch stop layer (16) covering the at least one first MOS (NMOS) transistor and the at least one second MOS (PMOS) transistor and having a second residual stress level different than the first residual stress level (layer 14 has a tensile stress and layer 16 has a compressive stress and hence layers 14 and 16 have different residual stress levels, refer to paragraph 0088 and 0089).

Regarding claim 34, Saitoh teaches (fig. 5) the entire claimed process of claim 32 above including the dielectric layer (19) includes contact openings therethrough for providing electrical connection to the at least one first (NMOS) MOS transistor and to the at least one second (PMOS) MOS transistor (refer to paragraph [0106]).

Regarding claim 35, Saitoh teaches (figs. 3A-3B) the entire claimed process of claim 32 above including forming the first layer (14) covering the at least one first MOS transistor (NMOS) and the at least one second MOS transistor (PMOS); forming a mask (15) on the at least one first MOS transistor (NMOS); removing the first layer (14) on the at least one second MOS transistor (PMOS, fig. 3B); and removing the mask (fig. 3B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 13, 21 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saitoh.

Regarding claims 13, 21 and 33 Saitoh teaches substantially the entire claimed structure of claims 12, 20 and 32 above except explicitly stating that the first and second etch stop layers have different thicknesses.

Parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of the first and second etch stop layers as claimed in order to form a CMOS transistor with improved electron mobility.

7. Claims 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng, US patent No., 6,762,085 in view of Saitoh.

Regarding claim 26, Zheng teaches a semiconductor device comprising: a semiconductor substrate (1); at least one PMOS transistor (40) and at least one NMOS transistor (30) in the semiconductor substrate (1); and a first etch-stop layer (14a)

covering the at least one PMOS transistor (40) and having a first residual stress level (inherent characteristics of the material) and a second etch-stop layer (4b) covering the at least one PMOS transistor (40) and the at least one NMOS transistor (30) and having a second residual stress level different than the first residual stress level (since the two etch stop layers are different they inherently have different stress level).

Zheng does not explicitly teach a dielectric layer on the at least one PMOS transistor and on the at least one NMOS transistors.

Saitoh teaches (fig. 5) the use of dielectric layer (19) to cover both the PMOS and NMOS transistor structures (fig. 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the dielectric layer taught by Saitoh in the structure of Zheng in order to provide insulation during subsequent integration of the CMOS device.

Regarding claim 27, Zheng teaches substantially the entire claimed structure of claim 26 above including the first and second etch-stop layers have different thickness (4b has a thickness range of 200 to 400 Ang, while 14a has a thickness range of 200-800 Ang).

Regarding claim 28, Zheng teaches substantially the entire claimed structure of claim 26 above including the dielectric layer includes contact openings therethrough for providing electrical connection to the at least one PMOS transistor and to the at least one NMOS transistor (refer to paragraph [0106], Saitoh).

Regarding claim 29, Zheng teaches substantially the entire claimed structure of claim 26 above except explicitly stating that the first and second etch-stop layers have opposite residual stress levels.

Saitoh teaches (fig. 5) first (14) and second (16) etch-stop layers having opposite residual stress levels (refer to paragraph [0088] and [0089]) in the structure of a CMOS device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the opposite residual stress level taught by Saitoh in the structure of Zheng in order to enhance the electron mobility of the device (paragraph [0020]).

Regarding claim 30, Zheng teaches substantially the entire claimed structure of claim 26 above including the first etch-stop layer has a negative residual stress level (compressive stress) above the at least one PMOS transistor, and the second etch-stop layer has a positive residual stress level (tensile stress) above the at least one NMOS transistor (refer to paragraph [0088] and [0089] of Saitoh).

8. Claims 17-19, 25 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saitoh in view of Zheng.

Regarding claim 17, Saitoh teaches substantially the entire claimed structure of claim 12 above except explicitly stating that the at least one first MOS transistor comprises PMOS transistors and the at least one second MOS transistor comprises NMOS transistors.

Zheng teaches (fig. 10) a CMOS device where a first layer (14a) covering the at least one first MOS transistor (40); and a second layer (4b) covering the at least one first MOS (40) transistor and the at least one second MOS transistor (30) and the at least one first MOS transistor comprises PMOS (40) transistors and the at least one second MOS transistor comprises NMOS (30) transistors.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the layers taught by Zheng in the structure of Saitoh in order to reduce the process cost of forming CMOS device (refer to abstract) and providing better insulation.

Regarding claim 18, Saitoh teaches substantially the entire claimed structure of claims 12 and 16 above including the first layer has a negative residual stress (compressive stress) level above the PMOS transistors, and the second layer has a positive residual stress (tensile stress) level above the NMOS transistors.

Regarding claims 19 and 25, Saitoh teaches substantially the entire claimed structure of claims 12 and 20 above including a zone formed by the second layer overlapping the first layer (the region where the compressive stress and the tensile stress intersect, the middle region of the CMOS device, refer to fig. 5) has a substantially zero residual stress level.

Regarding claim 31, Saitoh teaches substantially the entire claimed structure of claims 12, 19 and 30 above including a zone formed by the second layer overlapping the first layer (the region where the compressive stress and the tensile stress intersect,

the middle region of the CMOS device, refer to fig. 5) has a substantially zero residual stress level.

9. Claims 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saitoh in view of admitted prior art (APA).

Regarding claim 36, Saitoh teaches (fig. 5) substantially the entire claimed process of claim 32 above except explicitly stating performing a localized treatment of the first and second layers that overlap the at least one first MOS transistor for modifying the second residual stress level of the second layer.

APA teaches that ion implantation is used on nitride layer to improve either the operation of PMOS transistor or NMOS transistor (APA, specification page 2).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the treatment suggested by APA as claimed in the process of Saitoh in order to further enhance the mobility of the MOS transistors.

The combined process of Saitoh and APA would modify the second residual stress level of the second layer.

Regarding claim 37, Saitoh teaches (fig. 5) substantially the entire claimed process of claims 32 and 36 above including performing the localized treatment comprises implanting ions into the second layer (APA, specification page 2).

Regarding claim 38, Saitoh teaches substantially the entire claimed process of claims 36 and 37 above including germanium ions are implanted into the second layer (APA, specification page 2).

Response to Arguments

10. Applicant's arguments with respect to claims 12-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W. Owens

SAG
April 29, 2006

DOUGLAS W. OWENS
PRIMARY EXAMINER